WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device comprising:

epitaxially growing a silicon-germanium base on a collector;

thermally oxidizing the base to preferentially grow silicon dioxide on an upper surface of the base to form a germanium-enriched region in an upper region of the base;

removing the silicon dioxide; and

depositing an emitter overlying the base.

2. The method of claim 1 wherein the germanium-enriched region has a low level of lattice defects.

3. The method of claim 1 wherein prior to the step of thermally oxidizing, the silicon-germanium base comprises a graded doped silicon-germanium base or a stepped doped silicon-germanium base.

4. The method of claim 1 wherein prior to the step of thermally oxidizing, the silicon-germanium base comprises a uniformly doped silicon-germanium base.

5. The method of claim 1 wherein a concentration of germanium in the germanium-enriched region ranges from about 30 percent to about 75 percent relative to a concentration of silicon in the germanium-enriched region. .

6. The method of claim 1 wherein the step of thermally oxidizing the base comprises thermally oxidizing the base within a temperature range of about 700 to about 900 degrees Celsius.

7. The method of claim 1 wherein the germanium-enriched region contacts with the emitter.

8. The method of claim 1 wherein a concentration of germanium in the germanium-enriched region decreases abruptly from a concentration in the upper region of the base in a direction toward the collector.

9. The method of claim 1 wherein the step of thermally oxidizing the base further comprises thermally oxidizing the base to preferentially grow silicon dioxide on an upper surface of the base to form the germanium-enriched region adjacent the silicon dioxide.

10. The method of claim 1 further comprising annealing the semiconductor device to redistribute germanium atoms of the germanium-enriched region.

11. The method of claim 10 wherein the annealing step increases a germanium concentration in a region of the base proximate the germanium-enriched region.

12. The method of claim 1 wherein the silicon-germanium base comprises a silicon-germanium layer within a base.

13. A method of manufacturing a semiconductor device comprising:

forming a silicon-germanium base region, having a first upper surface, over a collector region;

reacting the base region along the upper surface to form a thermally grown oxide in the first upper surface;

removing the thermally grown oxide to expose a second upper surface of the base region; and

forming an emitter region over the base.

14. The method of claim 13 wherein the step of reacting the base region further comprises varying a germanium concentration such that the germanium concentration is greater near the second upper surface.

15. The method of claim 14 wherein the germanium concentration near the second surface is between about 30 percent and about 75 percent relative to the concentration of silicon near the second surface.

16. The method of claim 13 wherein the step of reacting the base region further comprises reacting the base region within a temperature range of about 700 to about 900 degrees Celsius.

17. A method of manufacturing a semiconductor device comprising:

forming a base on a silicon collector, wherein the base comprises a silicon-germanium layer proximate an upper surface thereof;

thermally oxidizing the silicon-germanium layer to form a germanium-enriched portion proximate the upper surface, wherein the germanium-enriched portion has a significantly greater germanium concentration than a remainder of the base, and

forming an emitter on the germanium-enriched portion.

18. The method of claim 17 wherein the germanium-enriched portion has a germanium concentration greater than about 30%.

19. A heterojunction bipolar transistor comprising:

a collector;

a base disposed above the collector, the base comprising a silicon-germanium layer;

a germanium-enriched region proximate an upper surface of the base and within the silicon-germanium layer; and

an emitter overlying the germanium-enriched region.

20. The heterojunction bipolar transistor of claim 19 wherein the germanium-enriched region creates a band-gap differential between the emitter and the base.

21. The heterojunction bipolar transistor of claim 19 wherein carrier mobility is greater in the germanium-enriched region than in the base.

22. The heterojunction bipolar transistor of claim 19 wherein the germanium-enriched region comprises a strained germanium-enriched region.

23. The heterojunction bipolar transistor of claim 19 wherein a germanium concentration in the germanium-enriched region ranges from about 30 percent to about 75 percent.

24. The heterojunction bipolar transistor of claim 19 wherein a germanium concentration is greater in the germanium-enriched region than in the silicon-germanium layer.

25. The heterojunction bipolar transistor of claim 19 having a valence band offset of greater than about 0.21 eV.

26. The heterojunction bipolar transistor of claim 19 wherein the germanium-enriched region has a relatively low level of lattice defects.

27. The heterojunction bipolar transistor of claim 19 wherein the base comprises a graded doped silicon-germanium base or a stepped doped silicon-germanium base.

28. The heterojunction bipolar transistor of claim 19 wherein the base comprises a uniformly doped silicon-germanium base.

29. The heterojunction bipolar transistor of claim 19 wherein the germanium-enriched region is in contact with the emitter.

30. The heterojunction bipolar transistor of claim 19 wherein a concentration of germanium in the germanium-enriched region decreases abruptly from a concentration proximate the upper surface in a direction toward the collector.

31. A bipolar junction semiconductor comprising:

a silicon substrate;

a collector disposed in the substrate;

a base disposed overlying the collector, wherein the base comprises a silicon-germanium portion;

a germanium-enriched region formed in the silicon-germanium portion, wherein a concentration of germanium in the germanium-enriched region is substantially greater than the concentration of germanium in the silicon-germanium portion; and

an emitter disposed overlying the germanium-enriched region

32. The bipolar junction semiconductor of claim 31 wherein the germanium-enriched region comprises a thermally oxidized enriched region.

33. The bipolar junction semiconductor of claim 31 wherein the germanium enriched region includes at least a 30% germanium concentration.